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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,787	01/30/2002	Masatoshi Hasegawa	ASAM.0038	4712

7590 12/17/2003

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,787	HASEGAWA ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *9-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-8 in Paper No. 7, filed 9/25/03 is acknowledged. Accordingly, claims 9-12 have been withdrawn from consideration as being drawn to a nonelected invention.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,269,036 to Shubat.

Regarding claim 1, Shubat discloses a semiconductor IC device (figure 5) comprising: an internal circuit (508) whose state of operation is controlled in response to an internal operation control signal (WL signal), a control circuit (516, 506, 514) for forming the internal operation control signal (figure 7B and 7C); wherein the control circuit has its inputs connected to a terminal to which an external operation control signal (CLK, EQ, and CCLK) is supplied (terminal to which a timing signal used exclusively for testing (TEST) is supplied (see figure 5), the control circuit being capable of providing control between a test mode and a normal

operation mode (see figures 5-7C), wherein, in the test mode (figure 7c), the internal operation control signal (WL) changes from a first state of control (low) to a second state of control (high) in response to a change of the external operation control signal from a first state to a second state (CCLK, EQ in figure 7C); and the internal signal is changed to the first state in response to the timing exclusively for testing (TEST; see figure 7C); and where in the normal operation mode (figure 7B), the internal signal is changed from a first to a second state and to a first state in response to the change of the external operation control signal to the first state (figure 7B).

Regarding claims 2 and 3, Shubat discloses that the external operation control signal consists of a clock signal (CLK) and a memory select signal (CCLK; EQ, column 5, lines 45-50; column 7 lines 20-24), and that the internal operation control signal changes levels in response to a change in levels of the memory select signal synchronized with a clock signal (see figures 7B and 7C; CCLK is automatically synchronized with CLK (figure 6A)).

Regarding claims 4 - 5, Shubat discloses that the memory circuit is a read/write cell includes a memory cell which has its selection terminal connected to a corresponding word line and its data terminal connected to a corresponding bit line (figure 1), where in correspondence with the first state of control of the internal operation control signal, the word line selection is terminated, and the bit line potential is reset (column 7, lines 15-25; column 8, line 50 – column 9, line 12), and where in response to the change of the internal operation control signal from the first to the second state, the word line selection is started, and write data is imparted to the bit line (column 7, lines 15-25; column 8, line 50-column 9, line 12).

Regarding claim 6, Shubat discloses that the terminal to which the test signal is supplied is a terminal provided on a semiconductor IC chip as a terminal used exclusively for the TEST

signal (column 5, lines 35-40 shows that circuit 502 is a semiconductor IC; figures 5 and 6 show a designated TEST terminal on the circuit).

4. Claims 1, 6, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,805,514 to Iwakiri.

Regarding claim 1, Iwakiri discloses an internal circuit (blocks 1-4 in figure 5; memory block of figure 13) whose state of operation is controlled in response to an internal operation control signal (S2, S3); an a control circuit (15, 35) for forming the internal operation control signal, wherein the control circuit has its inputs connected to a terminal to which an external operation control signal is supplied (Ck, St and addressing; see column 8, lines 37-67; column 10, line 61 – column 11, line 11; figure 1) and a terminal to which a timing used exclusively for testing (Ckt) is applied, the control circuit being capable of providing control between a test mode and a normal operation mode (from St), wherein, in the test mode, the internal operation control signal is changed from a first state to a second state in response to a change of the external control signal from a first state to a second state (from St and addressing), and changed back to a first state in response to the signal exclusively for testing (Ckt; see figure 2); and in normal mode, the internal control signal is changed from a first to a second state, and back to a first state in response to the external signal (CK; see figures 1 and 2; since St =0 in the normal mode, S2 and S3 would change states in correspondence with the CK signal).

Regarding claim 6, Iwakiri discloses that the timing signal used exclusively for testing is supplied to a terminal on an IC used exclusively for the timing signal (33; see column 5, lines 4-7).

Regarding claim 7, Iwakiri discloses that the control circuit has an input to which a mode signal (St) is supplied (figure 1), and effects the control operation in the test mode and the normal operation mode in response to the mode signal (St=0 corresponds to the normal mode, and St=1 corresponds to a test mode).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri in view of U.S. Patent No. 6,058,056 to Beffa et al.

Iwakiri discloses that the testing clock signal is set at a frequency lower than at the time of normal operation, and that the clock signal frequency can be optimized (column 5, lines 15-28).

Iwakiri fails to specify that the testing clock signal has a phase difference with the normal clock signal that corresponds to the frequency of the normal clock signal (i.e. a multiple of the testing clock frequency forms the normal clock frequency).

Beffa suggests using a testing signal corresponding to the frequency of the clock signal for normal operation (column 1, lines 40-67), and shows that it is feasible to do so by using a low frequency testing clock signal and applying a frequency multiplier circuit to form a testing clock having a frequency corresponding to a frequency of normal operation (see column 3, lines 22-32;

the low frequency testing signal corresponds to using a clock signal having a phase difference from the normal clock signal corresponding to the frequency of the normal clock signal.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the testing clock signal of Iwakiri, such that it has a phase difference with the normal clock signal corresponding to the frequency of the normal clock signal, as suggested by Beffa. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a testing clock having a frequency equivalent to the operating frequency of the memory, because doing so decreases the time and cost of testing the memory, and the testing signals then automatically satisfy the timing parameters of the memory (Beffa; column 1, lines 33- 67). Since Beffa shows that it is simple to generate a high frequency clock by supplying a low frequency clock, and then frequency multiplying (see column 3, lines 22-32), it is well within the purview of a person having ordinary skill in the art to follow the method of Beffa to generate the testing clock, and thus end up with a testing clock signal that has a phase difference with the normal clock corresponding to the frequency of the normal clock signal.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,034,904 to Kuromiya et al. discloses the formation of an internal RAS signal from an external RAS signal in a testing mode.

U.S. Patent No. 5,892,776 to Kumakura discloses a testing mode using a high frequency testing clock.

U.S. Patent No. 6,297,997 to Ohtani et al. discloses a memory in which an external RAS signal in conjunction with a testing clock controls internal memory operations.

U.S. Patent No. 6,061,285 to Tsukikawa discloses a memory system using a low frequency tester.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233 until 2/6/04, and (571)272-1690 after 2/6/04. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

ERIK J. KIELIN
PRIMARY EXAMINER